APPLICATION NOTE

THE 8 BIT HIGH SPEED, HIGH PERFORMANCE DATA CONVERTER TDA8708A VIDEO ADC

AN9308

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Application Note

The 8 bit high speed, high performance data converter TDA8708A video ADC

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Keywords

Evaluation board
8 bit, high speed data conversion
ADC & DAC
ADC with on–chip Clamp and AGC

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Summary :

An evaluation board is available for the TDA8708A 8 bit video A/D converter.
This board contains all the necessary circuits (including the TDA4690 Sync processor) for generating a line-locked sampling clock, ADC Clamp and ADC AGC control signals, from a CVBS video input.
External clocks and control signals are also allowed.
To allow quick evaluation of the TDA8708A performance, a TDA8702 8 bit D/A converter is also included on the board.
For ease of use, all necessary power supplies are generated by a Philips TDA3602 regulator, which needs only a +12V power source.
This report describes the functions and use of the board.

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1. INTRODUCTION

1.1 GENERAL DESCRIPTION

A new evaluation board has been developped for the 8 bit high speed, high performance, video A/D converter TDA8708A. The board contains all the necessary circuits for very simple demonstration of the TDA8708A capabilities in video applications, with a minimum of external equipment. Thanks to switches and supplementary BNC connectors, it allows a large flexibility, so that the TDA8708A, along with a TDA8702 8-bit DAC, may be extensively evaluated in a wide variety of applications (video applications or others).

1.2 FEATURES

- Evaluation of - TDA8708A or
  - TDA8708A plus TDA8702
- Only one +12V (up to +15V) +/- 10 % power supply.
- On board generation of +5V analog power supply and +5V digital power supply, for ADC, DAC and logic ICs, and of +8V power supply for TDA4690.
- On board power supply decoupling filters.
- 3 selectable video inputs to ADC via on-chip clamp and AGC circuits, or direct analog input to ADC.
- Two selectable clamping configurations for the video inputs : clamp on synchronization level (Mode I of TDA8708A) or clamp of black level on code 64 of TDA8708A (Mode II of TDA8708A).
- Selection between on-board generated clamp and AGC control pulses and external user-defined control pulses.
- Selection between on-board generated line-locked clock (13.5 MHz or 27 MHz) and external user-defined clocks, independantly for ADC and DAC.

- Selectable binary or two's complement 3-state TTL ADC outputs on connector CB1.

- All digital inputs and outputs are TTL compatible.

- All option selections by on-board switches.

Figure 1-1 shows the block diagram.
The boards are fully assembled and tested.

Note : To separate ADC and DAC the solder links TC1 to TC8 must be removed.

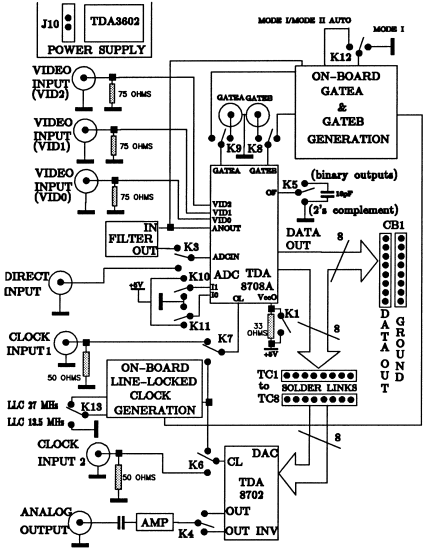


Figure 1–1 Block diagram of the application board

2. ANALOG INPUTS

The boards have two analog input options : video or direct input (see figure 2-1).

2.1 VIDEO INPUTS

Three video inputs (VID0, 1, 2) matched to 75 Ω allow to test the A/D converter using standard video signals (see figure 2-1). A clamp circuit and an A.G.C. are available in the TDA8708A ADC. So using these video inputs every video signal with a peak to peak amplitude between 0.6V and 1.5V can be converted with the best performances.

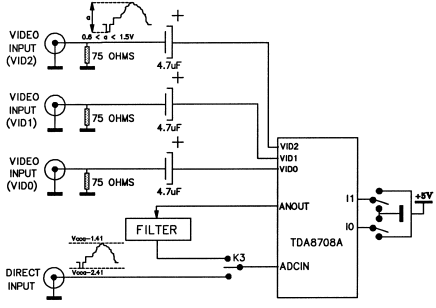


Figure 2-1 Analog input diagram

Note : The selection between the three video inputs is made by actuacting the switches K10 and K11 (see figure 2-2).

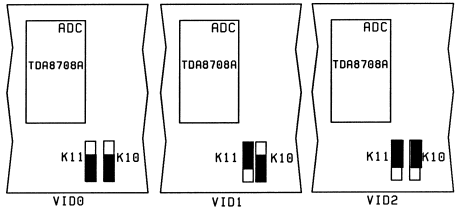


Figure 2-2 Video input selection

2.2 DIRECT INPUT

A direct input (ADCIN) allows to use the board for various applications. Using this input only the conversion part of the ADC is available. The input range is [Vcca-2.41,Vcca-1.41]. The analog input signal must be within and as close as possible to the maximum input range in order to use the maximum resolution of the ADC.

The selection between Vid-in and Aux-in is made by actuating the K3 switch.

3. CLOCK GENERATION, INPUTS AND TIMING ASPECTS

3.1 CLOCK ON-BOARD GENERATION SYSTEM

3.1.1 13.5 MHz line-locked clock

For an on-board clock generation system, we are using Philips TDA4690 Sync-Processor with Clock (SPC), which extracts all Sync signals from a CVBS input, and also generates a line-locked 13.5MHz TTL compatible clock. This clock is buffered by 74F86 XOR gates, which allow to optionally double the clock frequency, and may then be input to ADC and DAC.

Note : For all relevant information about TDA4690 application, please refer to Laboratory Report HVT/CR92001.

3.1.2 27 MHz line-locked clock

For most video applications, a 13.5 MHz ADC clock is considered sufficient, however, for those who intend to implement more complex signal treatment, such as interpolation, filtering,... a 27 MHz clock may be desirable.
To generate such a 27 MHz clock, the 13.5 MHz clock is buffered, then simply input in a 74F86 XOR gate, together with a 13.5 MHz clock delayed by about 27ns.
The 27ns delay is created by a LC-cell, chosen to obtain a duty cycle of approximately 50% for the 27MHz clock. (L = 6.8µH, C = 12pF).

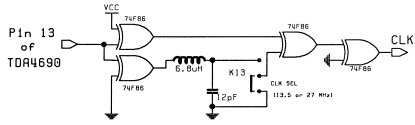


Figure 3-1 Clock frequency doubler

Selection between the two clocks (13.5 MHz and 27 MHz) is made via switch K13.

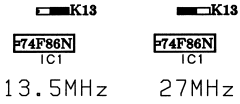


Figure 3-2 Change of on-board generated clock frequency

3.2 ADC AND DAC CLOCK INPUTS

Using switches K6 and K7, it is possible to choose between the following options :

- On-board generated line-locked clock (13.5 MHz or 27 MHz) input to both ADC and DAC.
- On-board generated line-locked clock (13.5 MHz or 27 MHz) input to ADC, user-defined external clock input to DAC (via connector J2).
- User-defined external clock input to ADC (via connector J3) and on-board generated line-locked clock (13.5 MHz or 27 MHz) input to DAC.
- User-defined external clock input to ADC (via connector J3) and user-defined external clock input to DAC (via connector J2).

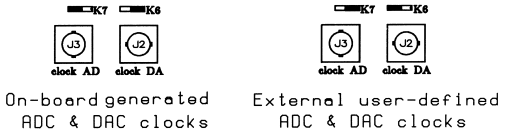


Figure 3–3 Selection of clock signals

Note : In order to get the best performances of the ADC the clock signal rise time must be superior to 2 ns. Otherwise some crosstalk could appear on the input signal.

3.3 CLOCK INPUTS AND TIMING ASPECTS

3.3.1 Timing of the TDA8708A

The analog input signal is latched on the rising edge of the clock and converted into digital data.

These data are available on the A/D outputs 20 nanoseconds (max) after the same rising edge of the clock. The output data are held during high level, high to low transition and low level of the clock and remain stable whatever change at the input.

So output data should only be used from 20ns minimally after the corresponding rising edge of the clock onwards.

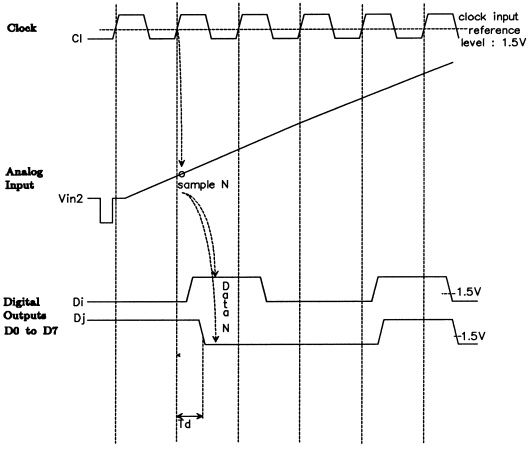


Figure 3–4 TDA8708A : Timing diagram

3.3.2 Timing of the TDA8702

The TDA 8702 is in a "transparent mode" when the clock is at low level : The analog output corresponds to the digital inputs at any moment. The converter latches the data on the rising edge of the clock. The analog output signal is constant during the whole high clock level and corresponds to the latched digital input data (the typical delay time input to 50% output, td is 3ns (see figure 3-5)). The converter becomes transparent again on the falling edge.

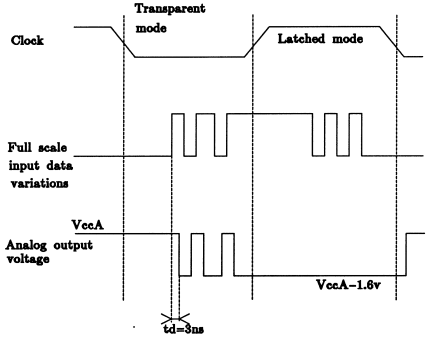


Figure 3-5 TDA8702 : Timing diagram

3.3.3 Timing of both converters

In this chapter a direct connection between the ADC outputs and the DAC inputs (TC1 to TC8) is set up. General timing aspect of the ADC and the DAC in one system can easily be derived from this discussion.

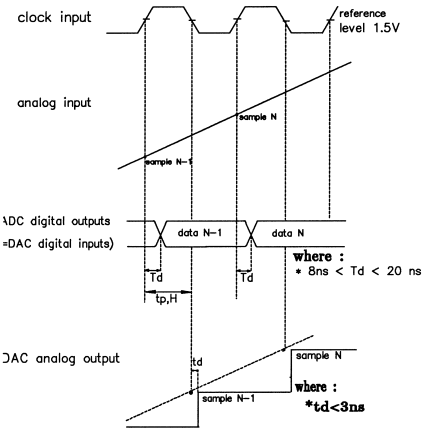


Figure 3–6
Timing diagram for a configuration where ADC outputs and DAC inputs are equal

At high clock frequencies, near the TDA 8702 limit of 30 Mhz the output data of the ADC TDA8708A might not have been entirely settled when the clock goes down, then causing the input data changes at the DAC during its transparent mode. this could cause undesired DAC output fluctuations (see fig. 3-7).

In practice to prevent the above mentionned undesired DAC output fluctuations, we recommend a delay between the clock signals of the ADC and the DAC (or, which might be a more realistic solution, between ADC output and DAC input) of minimum ($t_{p,H}-18$)ns and maximum 8 ns with formula : max(0,$t_{p,H}-18$)ns <delay < 8 ns.

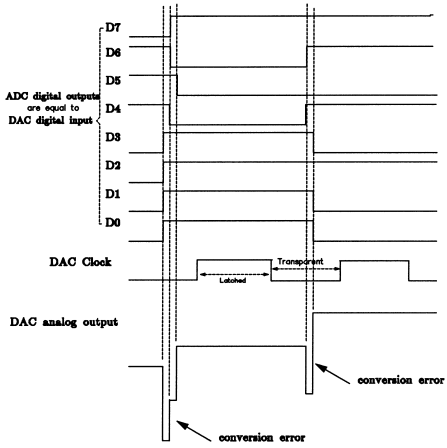


Figure 3–7 Example of conversion errors due to incorrect timing

Some ADC output bit transitions are faster than others. If these ADC output transitions enter the DAC inputs during the DAC's transparent mode (during clock low), then conversion errors, in the form of fast transients, appear at the DAC's output.

3.4 ON-BOARD GENERATED CLOCK SIGNAL SHAPE

In order to improve the TDA8708A characteristics, (harmonic suppression more than -55 dB), the on-board generated clock signal is connected to ADC and DAC via the following circuit :

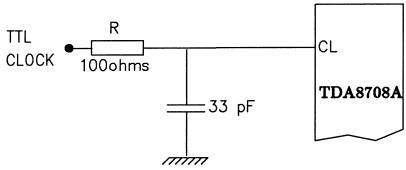


Figure 3-8 Change of clock input shape

Note : In case an external rectangular clock signal would be used, the same circuit should be implemented on the clock input.

4. TDA8708A : AGC AND CLAMP CONFIGURATIONS

4.1 TDA8708A AGC AND CLAMP THEORY OF OPERATION

The TDA8708A ADC includes clamp and AGC circuits that can operate in two different ways, referred to as Mode I and Mode II.

4.1.1 TDA8708A Mode I

The so-called 'Mode I' occurs when 'Gate A' (pin 27) and 'Gate B' (pin 26) TTL inputs are simultaneoulsy at high level (overlapping). It was designed as a 'start-up' mode, to roughly adjust a signal between codes 0 and 255 (full-scale) at the beginning of operation. Normally, for video signal inputs, the TDA8708A should then be switched to Mode II.

Note : Usually, when using TDA8708A with CVBS inputs, the 'Gate A' TTL pulse should be at high level during video Sync signal.

In Mode I, the TDA8708A AGC and clamp work in the following way:

- First, while 'Gate A' TTL input is at High level, the analog input is sampled, converted into binary and compared to code 0.
When this input is below code 0, the clamp capacitor (pin 24) is discharged with a I_{peak} current, so that the input is clamped up to 0.
When this input is above code 0, the clamp capacitor (pin 24) is charged with a 2.5 µA current, so that the input is clamped down to 0.

- Then, during the rest of the time, the analog input is sampled, converted to binary and compared to code 255. As long as this input is found superior to code 255, the AGC capacitor (pin 25) is discharged with a I_{peak} current, thus reducing the AGC gain. While this input is found below code 255, the AGC capacitor (pin 25) is charged with a 2.5 µA current, thus increasing the gain.

4.1.2 TDA8708A Mode II

The so-called 'Mode II' is the normal mode of operation for CVBS video signal inputs. It occurs when the High levels of 'Gate A' (pin 27) and 'Gate B' (pin 26) TTL inputs are not overlapping.

Note : Usually, when using TDA8708A with CVBS inputs, the 'Gate A' TTL input should be at high level during video Sync signal. the 'Gate B' TTL input should be at high level during the video black level.

In Mode II, the TDA8708A AGC and clamp work in the following way :

- First, while 'Gate A' TTL input is at High level, the analog input is sampled, converted into binary and compared to code 0.
When this input is below code 0, the AGC capacitor (pin 25) is discharged with a 2.5 µA current, so that the AGC gain is reduced.
When this input is above code 0, the AGC capacitor (pin 25) is charged with a 2.5 µA current, so that the AGC gain is increased.

- Second, while 'Gate B' TTL input is at High level, the analog input is sampled, converted into binary and compared to code 64.
When this input is below code 64, the clamp capacitor (pin 24) is discharged with a 50 µA current, so that the input is clamped up to 64.
When this input is above code 64, the clamp capacitor (pin 24) is charged with a 50 µA current, so that the input is clamped down to 0.

- Then, during the rest of the time, the analog input is sampled, converted to binary and compared to code 248. As long as this input is found superior to code 248, the AGC capacitor (pin 25) is discharged with a I_{peak} current, thus reducing the AGC gain. (This is called 'White-peak control').

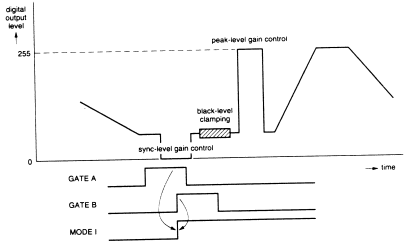
The practical effect of this operation in standard use ('Gate B' high during Black level, 'Gate A' high during Sync) is that :
1) The black level of the video input signal is clamped to code 64.
2) The AGC gain is adjusted so that the Sync tip is adjusted to code 0.

Note : this means that, for a standard composite video signal (sync = 30%,

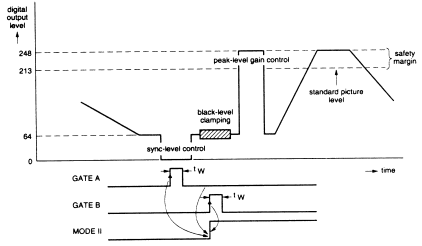
active video = 70 %), the video white level will reach the code :
64 + (70/30)x64 = 213.

Note : It is very important that on start-up the two control pulses Gate A and Gate B be present on the TDA8708A inputs, because otherwise the ADC may randomly lock in either Mode I or Mode II.

Note : for normal AGC and clamp behaviour, the minimum width for Gate A and Gate B pulses should be 2 µs.



Control mode 1.



Control mode 2.

Figure 4–1 AGC and clamp control signals

4.2 AGC GAIN RANGE

The AGC gain range is −4.5 dB, +6 dB, and the AGC amplification factor is 0 dB for a 1.33V input (peak to peak). The AGC total output swing is $1.33V_{p-p}$ (full−scale, from code 0 to code 255) on pin 19.

Note : for a nominal CVBS video signal (Sync = 30%, Video = 70%), in Mode II, the signal will be between codes 0 and 213, so the AGC output amplitude (on pin 19) will be in this case :

$$213/255 \times 1.33 = 1.10V_{p-p}$$

4.3 AGC AND CLAMP TIME CONSTANTS

The clamp and AGC time constants are controlled by choosing the values of the capacitors connected to pins 24 and 25 of the ADC.
The capacitor values which are advised for standard TV application are the following :
On pin 24 : C_{clamp} = 18 nF,
On pin 25 : C_{AGC} = 220nF,
On pins 16, 17 and 18 : C_{in} >= 2.2 µF

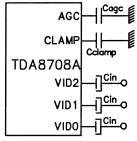


Figure 4−2 AGC and Clamp capacitors

This proposal is made so that the gain variation will be lower than 0.1 dB per field and the input variation due to the effect of input capacitive coupling will be lower than 1 LSB during one line.

Note : these values may vary according to specific application constraints.

The I_{peak} current is controlled by the R_{peak} resistor connected between ADC pin 28 and ground.

Note : When R_{peak} = 0 Ω, I_{peak} = 80 μA
In order not to unlock the AGC, it is advised not to exceed a value of 1 mA for I_{peak}, which corresponds to R_{peak} = 3.3 kΩ (typical values)

4.4 EXTERNAL CONTROL OF THE A.G.C.

An external control of the AGC can be used by forcing a voltage on pin 25 (AGC) instead of implementing the C_{AGC} capacitor. The voltage can vary between 2.8V (for a minimum gain of −4.5 dB) and 4V (for a maximum gain of +6 dB).

But in such an application one must take care of the temperature dependance, and so include the AGC voltage source in a regulation loop (the AGC output information (pin 19) or the digital data can be used).
Furthermore in this case the pin 28 (R_{peak}) must be connected directly to analog ground in order to have the minimum I_{peak} current (typically 80 μA).

4.5 AGC AND CLAMP CONTROL PULSES ON-BOARD GENERATION

For the on-board generation of AGC and clamp control pulses (Gate A and Gate B), we are using extensively the possibilities of the TDA4690 SPC, which, from a composite video input (pin 20), can regenerate a TTL compatible composite sync (pin 9), a TTL compatible positive-going horizontal sync (pin 11), and a TTL compatible positive-going vertical sync (pin 10).
It is also outputing (on pin 4) information on the presence of a signal at its input, and a 13.5 MHz line-locked clock on pin 13.

Note : for complete information on TDA4690, please refer to Laboratory Report HVT/CR92001.

We AC-coupled the composite input of TDA4690 (pin 20) to the ANOUT

pin of TDA8708A (pin 19) via a 100nF capacitor.
This ANOUT pin being the output of TDA8708A AGC, signal amplitude is maximum there. Moreover, whichever video input is used, there is always a signal input in TDA4690.

We could not use the CS output of TDA4690 (pin 9) for Gate A information, (during sync) because it was too large and overlapped black level.
So we chose to use HS output (horizontal sync, pin 11 of TDA4690) as a Gate A signal (it is possible to position HOUT right into the sync pulse by connecting pin 14 of TDA4690 to Ground).

For GATE B control pulse, we used the CS (composite sync) of TDA4690 to trigger a 74HCT123 monostable multivibrator (IC2), which allow us to choose quite finely the width of Gate B pulse. To make sure the Gate B pulse would end in the black level, after the burst (in order to have better accuracy of the ADC clamp), we used a 2.7 nF capacitor (C8) to delay CS at the input of the 74HCT123.
The discrete components values chosen (C7 = 1 nF and R7 = 6.8 kΩ) are given for a pulse width of approximately 3 µs at the output of the multivibrator.

Note : it could have been possible to use HS output for the trigger, but HS is PLL-generated in TDA4690, and during field backfly some erroneous information (such as clamp on code 0) might be given to TDA8708A.

Switch K12 allows to select between Mode I and Mode II operations, by controlling the multiplexer IC3.

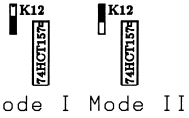
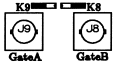


Figure 4-3 Switch position for Mode I or Mode II operation

We could have done without IC3 but a further advantage of the MUX is that, by connecting pin SI of the TDA4690 (pin 4), which indicates if a signal is there or not, we can automatically switch the TDA8708A between Mode I (when no signal is recognized at the output of the AGC), where the gain is roughly increased, and Mode II (when a signal is seen at the output of the AGC) where the clamp level and gain are more finely adjusted.

4.6 SELECTION OF GATE A AND GATE B SIGNALS

On-board switches K8 and K9 allow users to choose between on-board generated Gate A and Gate B pulses (in Mode I or Mode II) and external user-defined control pulses.



On-board generated GATEA & GATEB pulses

External user-defined GATEA & GATEB pulses

Figure 4-4 Selection of GateA and GateB control pulses

5. TDA8708A LOWPASS FILTER

A low-pass filter must be implemented between pins 19 and 20 of the TDA8708A ADC, that is between the AGC output and the ADC input. This filter, which serves as an antialiasing filter, is also used to ensure good clock rejection.

5.1 FILTER REQUIREMENTS

Since the TDA8708A is mainly used in video applications, with CVBS bandwidth about 6 MHz, filters have been designed to ensure good video performance at reasonable cost.
Clock rejection should reach 40 dB, while ripple for a video system should not exceed 0.3 dB.

The AGC output swing is 1.33Vp-p, while the ADC total input range is 1Vp-p (from code 0 to code 255), so filters must present a 0.75 attenuation factor.
Moreover, the load impedance of the AGC must be high enough to avoid any degradation of the differential gain and phase of the IC.
These considerations have driven us to choose a 680Ω resistor as filter source resistor and a 2.2kΩ as load resistor.
Please note that the filter must be referenced to VccA (analog +5V supply).

The other components of the filters have been chosen accordingly to ensure suitable video performance.

5.2 EVALUATION BOARD FILTER

The filter we implemented on the evaluation board and its performance are shown hereafter.

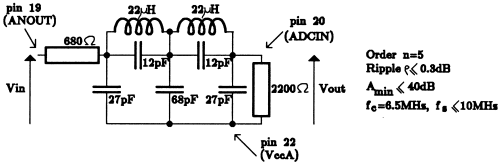
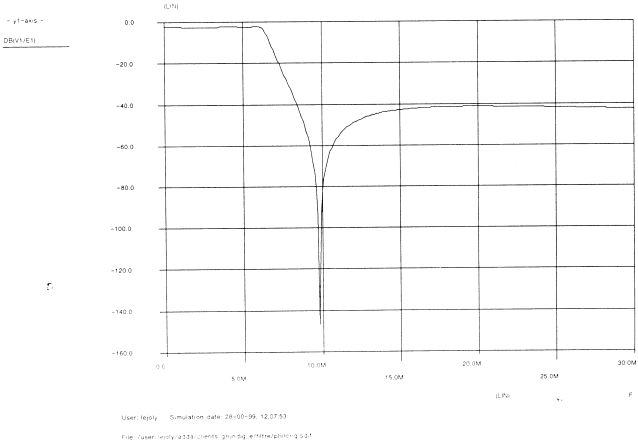


Figure 5-1 High-end low-pass filter, implemented on the evaluation board



5.3 ALTERNATE FILTER

For those customers who may want to reduce costs, we show hereafter an alternate filter solution which we think is a good compromise for an ADC clocked at 27MHz and above.

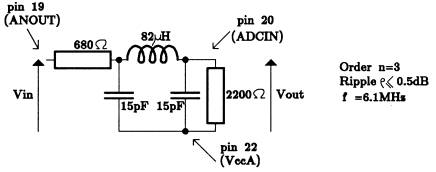
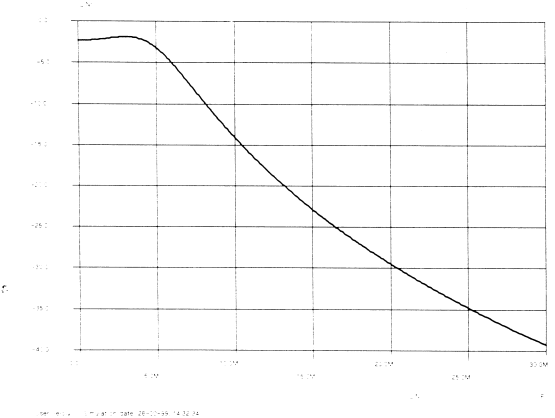


Figure 5-2 Low-cost low-pass filter



6. TDA8708A DIGITAL OUTPUTS

6.1 OUTPUT FORMAT SELECTION

K5 allows to select the binary or two's complement (active low) format of the ADC output.

6.2 DIGITAL DATA OUTPUTS

The digital outputs of the TDA 8708A are directly fed to a connector (CB1, see figure 6-1) which provides :

- the 8 bits at TTL level (D0...D7)
- the digital ground

and allows to connect to the board a data processing system.

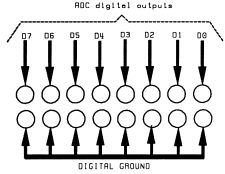


Figure 6-1 Connector CB1 pinning

Note : to avoid glitches that may appear on the output data of TDA8708A, (in case the digital voltage supply is not properly designed), a 33Ω resistor has been added between the digital supply source and the VccO pin of the ADC (pin 7). Jumper K1 allows users to short-circuit this resistor if needed.

7. CONNEXION BETWEEN ADC AND DAC

On the evaluation board the contacts TC1 to TC8 have been connected by solder links under the board. To separate the ADC and DAC or to insert a data processing system the solder links must be taken away.

8. THE ANALOG OUTPUTS OF THE DAC TDA 8702

The TDA8702 DAC has two complementary outputs : $\overline{\text{VOUT}}$ and VOUT. Figure 8-1 gives an internal equivalent configuration diagram.

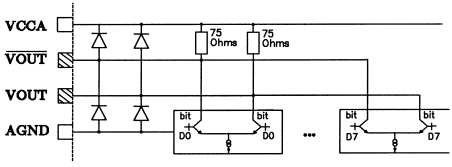


Figure 8-1 TDA8702 output pins configuration diagram

On the application board the K4 switch allows to select between VOUT or $\overline{\text{VOUT}}$.
The output impedance is 75 Ω.
The output voltage amplitude depends on the load impedance (see figure 8-2).

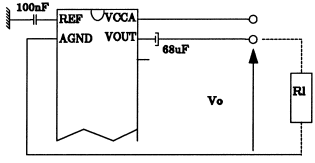


Figure 8-2 Output load

We find through a 68 µf capacitor :

$$Vo = \frac{\text{AC amplitude of VOUT x R1}}{\text{R1 + 75}}$$

Vo_{max}=0.8V if Rl=75Ω
Vo_{max}=1.6V if Rl is high impedance.

However on the board we added a transistor stage to output nominal amplitude video signals on 75Ω load, for direct plug-in into a TV SCART connector.

Note : More information on TDA8702 application may be found in Laboratory Report FTV/8902.

9. POWER SUPPLY AND PRINTED CIRCUIT

9.1 EVALUATION BOARD POWER SUPPLIES

We used the Philips TDA3602 regulator to generate all the supply voltages needed by the board from a single +12V supply (It can be used with a power supply up to +15V without any problem).

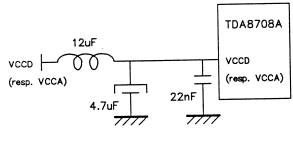
We are using TDA3602 in its minimal application setup, using the +8V regulator REG1 for TDA4690 supply, REG2 as +5V supply of all the digital parts (including the digital supplies of ADC and DAC, and TDA4690), REG3 as +5V supply for all the analog parts, including the analog supplies of ADC and DAC.

When appliable, we followed the advice provided below, especially we took care to separate as much as possible the analog and digital ground planes, connecting them only at the +12V supply and in one point under the ADC.

9.2 GENERAL RULES

It is necessary to have a good filtering of the power supply and to separate the printed wiring of the analog power supply VccA and digital power supply VccD.

As decoupling circuit of the analog and digital power supplies you should find a choke (about 12 µH) and two capacitors of 4.7 µF (close to the power supply point) and 22 nF (as close as possible to the component) as described below :



By the same way it is very important to separate the analog ground and the digital ground and to avoid the ground loops.

Remark : A 0,01 µF nonpolarized bypass capacitor can be added between analog and digital commons at the unit or both grounds must be joined under the ADC.

The printed wiring of the clock signals and of the data must be as short as possible and the printed wiring of the power supply and of the grounds must be wide.

Coupling between digital signal paths and the analog inputs must be minimized.

In case of a doubled sided PC board the component side would if possible be dedicated to the ground plane and the other side to the signal and power runs.

10. EVALUATION BOARD AVAILABILITY

Layout (scale 1/1), films and mounted P.C.B board are available on request.

11. APPENDIX

A / TDA8708A evaluation board

1/ Electric diagram

2/ Block diagram and switch position

3/ Component implantation

4/ Layout

5/ List of components

6/ References

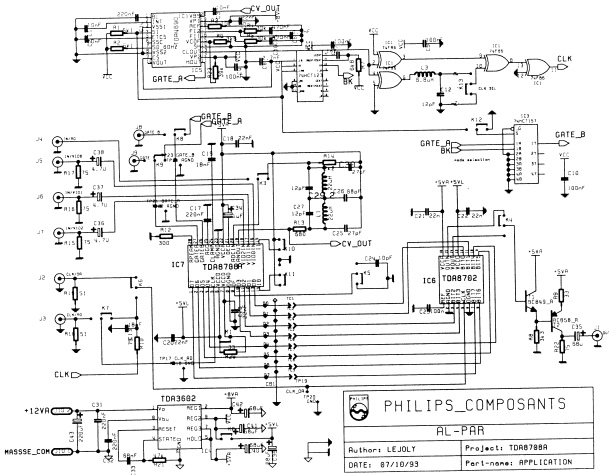


Figure 11–1 Electric diagram

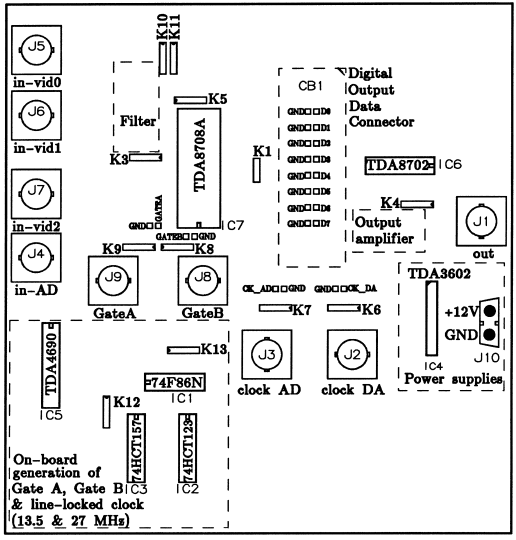


Figure 11–2 Block diagram

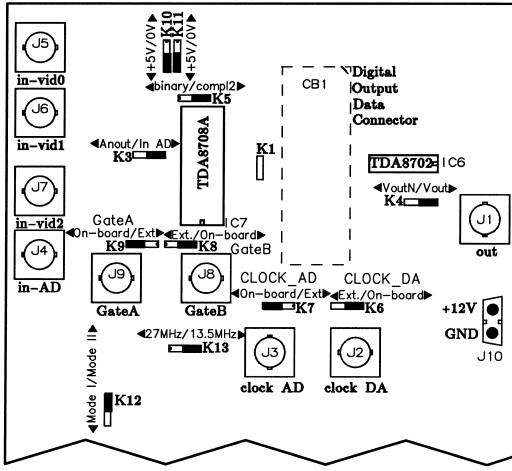


Figure 11–3 Switch position

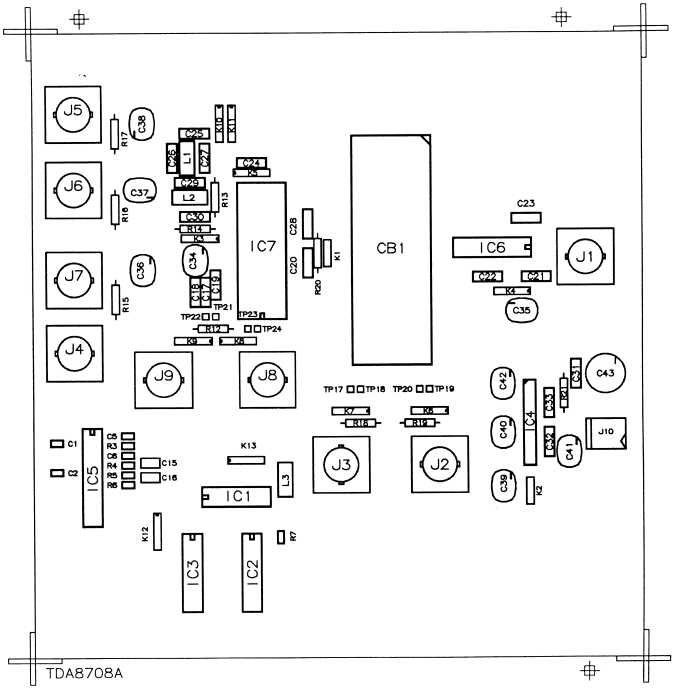


Figure 11–4 Component Implantation (Side 1)

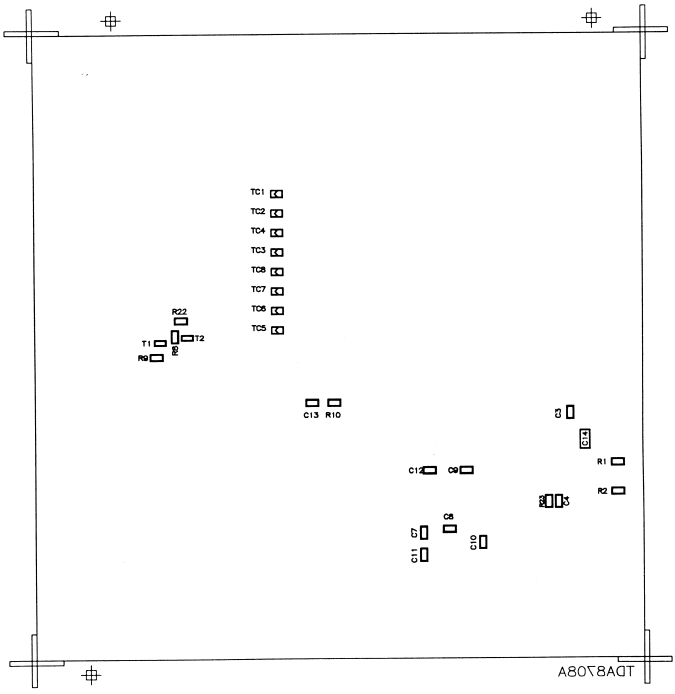


Figure 11–5 Component Implantation (Side 2)

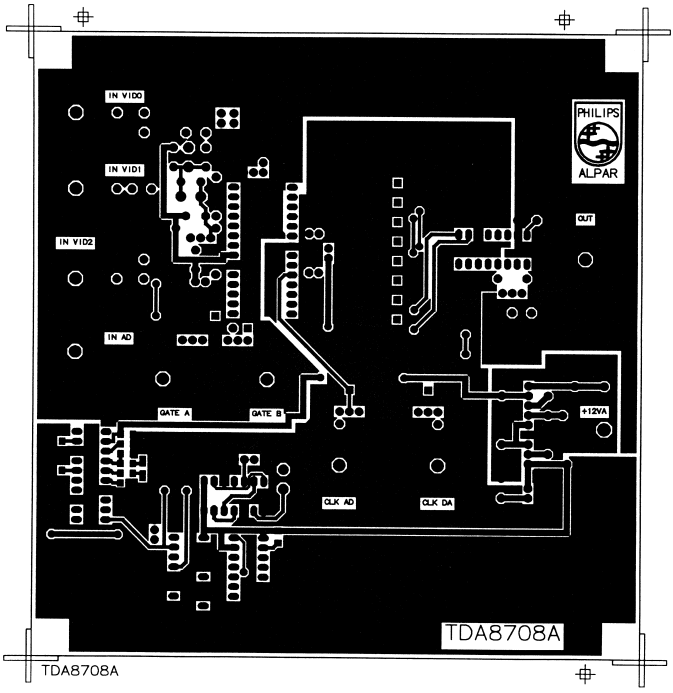


Figure 11–6 Layout (Side 1)

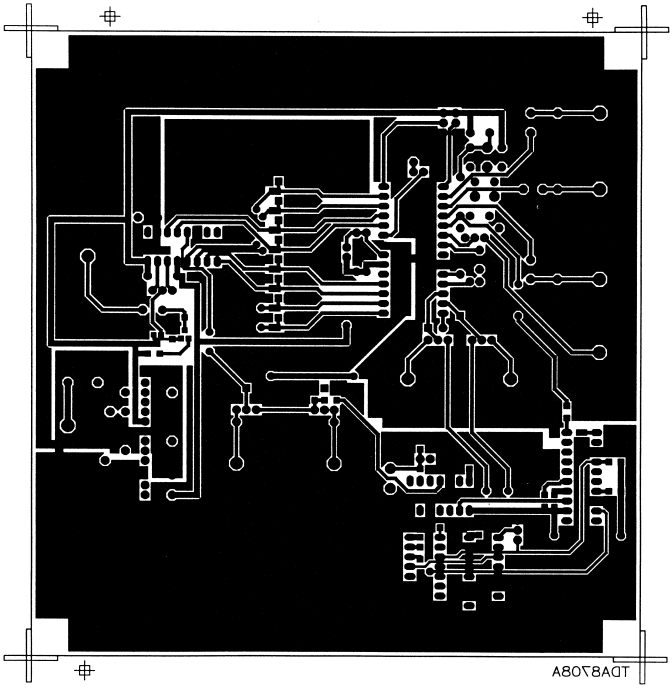


Figure 11–7 Layout (Side 2)

LIST OF COMPONENTS :

Resistors :

R1 : 5.1 kΩ
R2 : 5.1 kΩ
R3 : 10 kΩ
R4 : 30 kΩ
R5 : 30 kΩ
R6 : 3.6 kΩ

R7 : 75 Ω
R8 : 75 Ω
R9 : 100 Ω
R10 : 1 kΩ
R12 : 750 Ω
R13 : 100 Ω
R14 : 47 Ω
R15 : 75 Ω
R16 : 75 Ω
R17 : 75 Ω
R18 : 100 Ω
R19 : 75 Ω
R20 : 75 Ω
R21 : 75 Ω
R22 : 100 Ω
R23 : 39 kΩ

Capacitors :

C1 : 10 nF
C2 : 10 nF
C3 : 10 nF
C4 : 100 nF
C5 : 22 nF
C6 : 1.5 nF
C7 : 100 nF
C8 : 2.7 nF
C9 : 100 nF
C10 : 100 nF
C11 : 1 nF
C12 : 12 pF
C13 : 18 pF
C14 : 220 nF
C15 : 470 nF
C16 : 470 nF
C17 : 220 nF
C18 : 22 nF
C19 : 18 nF
C20 : 22 nF
C21 : 22 nF
C22 : 22 nF
C23 : 100 nF
C24 : 10 pF
C25 : 27 pF
C26 : 68 pF
C27 : 12 pF
C28 : 22 nF
C29 : 12 pF
C30 : 27 pF
C31 : 220 nF
C32 : 220 nF
C33 : 68 nF
C34 : 1 uF
C35 : 68 uF
C36 : 4.7 uF
C37 : 4.7 uF
C38 : 4.7 uF
C39 : 68 uF
C40 : 68 uF
C41 : 68 uF
C42 : 68 uF
C43 : 220 uF

Integrated circuits :

IC1 : 74F86
IC2 : 74HCT123
IC3 : 74HCT157
IC4 : TDA3602
IC5 : TDA4690
IC6 : TDA8702

IC7 : TDA8708A

Selfs :

L1 , L2 : 22 µH
L3 : 6.8 µH